What is claimed:

1. A method for forming a wafer level chip scale semiconductor package, the method comprising the steps of:

   a) providing a semiconductor wafer having a surface with a plurality of pads, wherein each of the pads has a conductor extending a first predetermined distance away from the surface;

   b) forming a layer of conductive etch resistant material on free ends of the conductors;

   c) disposing electrically insulating material on the surface of the semiconductor wafer, wherein the layer of electrically insulating material has an exposed surface a second predetermined distance from the surface of the semiconductor wafer, wherein the second predetermined distance is less than the first predetermined distance, and wherein portions of the electrically insulating material are disposed on the layer of conductive etch resistant material and on side surfaces of at least some of the conductors; and

   d) removing substantially all the portions of the electrically insulating material disposed on the layer of conductive etch resistant material and on the side surfaces of some of the conductors.

2. A method in accordance with claim 1 further comprising the steps of:

   e) disposing reflowable material on the conductive etch resistant layer on the free ends of the conductors: and

f) reflowing the semiconductor wafer causing the feflowable material to adhere to the conductive etch resistant layer and at least some of the side surfaces of the conductors.

3. A method in accordance with claim 1 wherein step (b) comprises the step of depositing the conductive etch resistant material on the free ends of the conductors.

4. A method in accordance with claim 3 wherein step (b) comprises the step of depositing gold.

5. A method in accordance with claim 3 wherein step (b) comprises the step of depositing solder.

6. A method in accordance with claim 3 wherein step (b) comprises the step of depositing a layer of nickel, and subsequently depositing a layer of gold on the layer of nickel.

7. A method in accordance with claim 1 wherein step (b) comprises the step of plating etch resistant material on the free ends of the conductors.

8. A method in accordance with claim 1 wherein step (c) comprises the step of dispensing the electrically insulating material with an extrusion coating process.

9. A method in accordance with claim 1 wherein step (c) comprises a single extruding step.

10. A method in accordance with claim 1 wherein step (c) comprises the step of spin coating the layer of electrically insulating material on the surface of the semiconductor wafer.

11. A method in accordance with claim 10 wherein step (c) comprises the step of spin coating one of the coating materials from the group including underfill coating materials and photo imageable materials.

12. A method in accordance with claim 1 wherein step (c) comprises the step of molding the layer of electrically insulating material on the surface of the semiconductor wafer using release film.

13. A method in accordance with claim 1 wherein step (d) comprises the step of plasma etching.

14. A method in accordance with claim 1 wherein step (d) comprises the step of employing at least one laser for etching.

15. A method in accordance with claim 1 wherein step (d) comprises the step of employing a media deflasher for etching.

16. A method in accordance with claim 1 wherein step (e) comprises the step of printing deposits of solder.

17. A method in accordance with claim 1 further comprising, after step (c) and before step (d), the step of curing the electrically insulating material.

18. A method in accordance with claim 17, after step (c) and before the step of curing the electrically insulating material, comprising the step of cleaning the portions of the electrically insulating material disposed on the layer of conductive etch resistant material.

19. A method in accordance with claim 18 wherein the step of cleaning comprises the step of:

applying release film on the layer of conductive etch resistant material; and

removing the release film.

20. A method in accordance with claim 18 wherein the step of cleaning comprises the step of laser cleaning.

21. A wafer level chip scale package comprising;

a semiconductor die having a plurality of pads on a surface;

conductors coupled to and extending a first predetermined distance from the surface of the semiconductor die;

an etch resistant layer on free ends of the conductors;

a layer of insulation on the surface, the layer of insulation having an exposed surface a second predetermined distance from the surface of the semiconductor die, wherein the second predetermined distance is less than the first predetermined distance; and

reflowable material attached to the etch resistant layer and to at least portions of side surfaces of substantially all of the conductors.

22. A wafer level chip scale package in accordance with claim 21 wherein the conductors comprise copper conductors.

23. A wafer level chip scale package in accordance with claim 22 wherein each of the copper conductors comprise a plurality of plated copper layers.

24. A wafer level chip scale package in accordance with claim 21 wherein the etch resistant layer comprises a layer of gold.

25. A wafer level chip scale package in accordance with claim 21 wherein the etch resistant layer comprises a layer of nickel with a layer of gold thereon.

26. A wafer level chip scale package in accordance with claim 25 wherein the thickness of the layer of gold is less than the difference between the first predetermined distance and the second predetermined distance.

27. A wafer level chip scale package in accordance with claim 21 wherein the layer of insulation comprises a material selected from the group including mold compound,

encapsulant epoxy, underfill coating, and photo imageable material, such as benzocyclobutene (BCB) or polyimide.

28. A wafer level chip scale package in accordance with claim 21 wherein the reflowable material comprises solder.

29. A wafer level chip scale package in accordance with claim 28 wherein the solder comprises eutectic solder.

30. A method for forming a wafer level chip scale semiconductor package, the method comprising the steps of:

(a) providing a semiconductor wafer having a surface with a plurality of pads, wherein each of the pads has a conductor extending a first predetermined distance away from the surface;

(b) disposing reflowable material on free ends of the conductors;

(c) disposing electrically insulating material on the surface of the semiconductor wafer, wherein the layer of electrically insulating material has an exposed surface a second predetermined distance from the surface of the semiconductor wafer, wherein the second predetermined distance is greater than the first predetermined distance; and

(d) selectively removing at least a portion of the electrically insulating material such that the exposed surface is a third predetermined distance from the semiconductor wafer, wherein the third predetermined distance is greater than the first predetermined distance and less than the second predetermined distance.

31. A method in accordance with claim 30 further comprising the step of:

(e) reflowing the semiconductor wafer causing the reflowable material to melt and reform a surface having reduced oxide thereon.

32. A method in accordance with claim 30 after step (a) and before step (b) comprising the step of depositing conductive etch resistant material on the free ends of the conductors, and wherein step (b) comprises the step of disposing reflowable material on the etch resistant material.

33. A method in accordance with claim 32 wherein the step of depositing conductive etch resistant material comprises the step of depositing gold.

34. A method in accordance with claim 30 after step (a) and before step (b) comprising the step of plating etch resistant material on the free ends of the conductors.

35. A method in accordance with claim 30 wherein step (b) comprises the step of printing deposits of reflowable material on the free ends of the conductors.

36. A method in accordance with claim 30 wherein step (b) comprises the step of printing solder on the free ends of the conductors.

37. A method in accordance with claim 30 wherein step (b) comprises the step of attaching solder balls to the free ends of the conductors.

38. A method in accordance with claim 30 after step (b) comprising the step of reflowing the semiconductor wafer.

39. A method in accordance with claim 30 wherein step (c) comprises the step of dispensing the electrically insulating material using an extrusion coating process.

40. A method in accordance with claim 30 wherein step (c) comprises a single dispensing step.

41. A method in accordance with claim 30 wherein step (c) comprises the step of spin coating the layer of electrically insulating material on the surface of the semiconductor wafer.

42. A method in accordance with claim 41 wherein step (c) comprises the step of spin coating a material selected from the group consisting of underfill coating materials and photo imageable materials.

43. A method in accordance with claim 30 wherein step (c) comprises the step of molding the layer of electrically insulating material on the surface of the semiconductor wafer using release film.

44. A method in accordance with claim 30 wherein step (d) comprises the step of plasma etching.

45. A method in accordance with claim 30 wherein step (d) comprises the step of employing at least one laser.

46. A method in accordance with claim 30 wherein step (d) comprises the step of employing a media deflasher.

47. A method in accordance with claim 30 further comprising, after step (c) and before step (d), the step of curing the electrically insulating material.

48. A method in accordance with claim 30, after step (b) and before step (d) comprising the step of cleaning the semiconductor wafer.

49. A method in accordance with claim 48 wherein the step of cleaning comprises the step of laser cleaning.

50. A wafer level chip scale package comprising:

a semiconductor die having a plurality of pads on a surface;

conductors coupled to and extending a first predetermined distance from the surface of the semiconductor die;

reflowable material attached to the free ends of the conductors; and

a layer of insulation on the surface of the semiconductor die and surrounding the conductors, the layer of insulation having an exposed surface a second predetermined distance from the surface of the semiconductor die, wherein the second predetermined distance is greater than the first predetermined distance.

51. A wafer level chip scale package in accordance with claim 50 further comprising an etch resistant layer between the free ends of the conductors and the reflowable material.

52. A wafer level chip scale package in accordance with claim 50 wherein the conductors comprise copper conductors.

53. A wafer level chip scale package in accordance with claim 52 wherein the copper conductors comprise a plurality of plated copper layers.

54. A wafer level chip scale package in accordance with claim 51 wherein the etch resistant layer comprises a layer of gold.

55. A wafer level chip scale package in accordance with claim 51 wherein the etch resistant layer comprises a layer of solder.

56. A wafer level chip scale package in accordance with claim 50 wherein the layer of insulation comprises a material selected from the group including mold compound, encapsulant epoxy, underfill coating, and photo imageable material, such as benzocyclobutene (BCB) or polyimide.

57. A wafer level chip scale package in accordance with claim 50 wherein the reflowable material comprises solder.

58. A wafer level chip scale package in accordance with claim 58 wherein the solder comprises eutectic solder.